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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,775	12/08/2003	Sung-Kwon Lee	P69355US0	2372

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EXAMINER	
NGUYEN, THANH T	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 09/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/728,775	LEE ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-35 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) 1-3,5-14,17-19,21-28 and 30-35 is/are rejected.

7)☒ Claim(s) 4,15,16,20 and 29 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/8/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d).

Information Disclosure Statement

The information disclosure statement filed on 12/8/03 has been considered.

Oath/Declaration

Oath/Declaration filed on 12/8/03 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ohuchi et al. (U.S. Patent No. 6,576,562).

Referring to figures 1A-1I, Ohuchi et al. teaches a method for fabricating a semiconductor device, comprising the steps of:

Forming a hard mask insulation layer (104) on an etch target layer (103);

Forming a hard mask sacrificial layer (105) on the hard mask insulation layer;

Forming an anti-reflective coating layer (106) on the hard mask sacrificial layer (meeting claims 18, 34)

Coating a photoresist (107) on the hard mask insulation layer;

Selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern (see figure 1E);

Etching the anti-reflective coating layer (see figure 1F) by using the photoresist pattern as an etch mask (meeting claim 18);

Selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width (see figure 1G);

Removing the photoresist pattern and the antireflective coating layer (see figure 1F-1H, meeting claim 18);

Etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width (see figure 1H); and

Etching the etch target layer (103) by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width (see figure 1I), wherein the first width (see figure 1E) is wider than the fourth width (see figure 1I).

Regarding to claims 2, 28, etch target layer is a conductive layer (polysilicon) and the line pattern is one of a bit line, a word line and a metal line (103).

Regarding to claims 3, 19, 27, photoresist is use one of ArF or F_2 photolithography (see col. 14, lines 42-54).

Regarding to claims 6, 30, the sacrificial hard mask is removed at the step of removing etch target (conductive) layer (see figure 1H-1I).

Claims 1-2, 6, 7-9, 13, 15, 18, 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Chan et al. (U.S. Patent No. 6,764,903).

Referring to figures 1-6, Chan et al. teaches a method for fabricating a semiconductor device, comprising the steps of:

Forming a hard mask insulation layer (16) on an etch target layer (14);

Forming a hard mask sacrificial layer (18) on the hard mask insulation layer;

Forming an anti-reflective coating layer (20) on the hard mask sacrificial layer (meeting claims 18, 34)

Coating a photoresist (22) on the hard mask insulation layer;

Selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern (see figure 1);

Etching the anti-reflective coating layer (see figure 2) by using the photoresist pattern as an etch mask (meeting claim 18);

Selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width (see figures 2-3);

Removing the photoresist pattern and the antireflective coating layer (see figure 4, meeting claim 18);

Etching the hard mask insulation layer by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width (see figure 5); and

Etching the etch target layer (see figure 6) by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width (see figure 6), wherein the first width (see figure 1) is wider than the fourth width (see figure 6).

Regarding to claims 2, 28, etch target layer is a conductive layer (polysilicon) and the line pattern is one of a bit line, a word line and a metal line (14).

Regarding to claims 6, 30, the sacrificial hard mask is removed at the step of removing etch target (conductive) layer (see figure 5-6).

Regarding to claims 7-8, 22, 31-32, the hard mask sacrificial layer and the target layer are made of (see col. 3, lines 46-58).

Regarding to claims 9, 33, hard mask sacrificial layer is made of an oxide-based material, nitride-based material or an oxynitride based material (see col. 3, lines 37-45).

Regarding to claim 13, etching the hard mask sacrificial layer by using a chlorine-based gas is used as a main etch gas if the hard mask sacrificial layer is made of polysilicon or titanium and one of oxygen (O_2) gas and carbon fluoride (CF) gas is added to the main etch gas to control an etch profile (see col. 5, lines 6-25).

Regarding to claim 15, etching the hard mask insulation layer by using plasma containing a mixed gas of CF_4, CHF_3, C_2H_4, He, Ar, and O_2 is used if the hard mask insulation layer is made of nitride-based material (see col. 5, lines 6-25).

Regarding to claim 23, the antireflective coating layer is made of organic material (20, see col. 3, lines 59-65).

Regarding to claim 24, etching the antireflective layer by using plasma containing missed gas of Cl_2 and Ar (see col. 4, lines 15-37).

Claims 1-2, 6, 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (U.S. Patent No. 6,171940).

Referring to figures 1-6, Huang et al. teaches a method for fabricating a semiconductor device, comprising the steps of:

Forming a hard mask insulation layer (40) on an etch target layer (30);

Forming a hard mask sacrificial layer (50) on the hard mask insulation layer;

Coating a photoresist (60) on the hard mask insulation layer;

Selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern (see figure 1);

Selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width (see figure 2);

Removing the photoresist pattern (see figure 3-4);

Etching the hard mask insulation layer (see figure 3) by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width (see figure 3); and

Etching the etch target layer (see figure 4) by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width (see figure 4), wherein the first width (see figure 1) is wider than the fourth width (see figure 4).

Regarding to claims 2, 28, etch target layer is a conductive layer (polysilicon) and the line pattern is one of a bit line, a word line and a metal line (30).

Regarding to claims 6, 30, the sacrificial hard mask is removed at the step of removing etch target (conductive) layer (see figure 3-4).

Regarding to claims 9, 33, hard mask sacrificial layer is made of an oxide-based material, nitride-based material or an oxynitride based material (see col. 2, lines 62-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 5-14, 17-19, 21-28, 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. (U.S. Patent No. 6,171940) or Chan et al. (6,764,903) as applied to claims 1-2, 6-9 above in view of Aminpur et al. (U.S. Patent No. 6,482726), Ohuchi et al. (U.S. Patent No. 6,576,562), Nallan et al. (U.S. Patent No. 6440870) and Blosse (U.S. Patent No. 6682996).

Referring to figures 1-6, Huang et al. teaches a method for fabricating a semiconductor device, comprising the steps of:

Forming a hard mask insulation layer (40) on an etch target layer (30);

Forming a hard mask sacrificial layer (50) on the hard mask insulation layer;

Coating a photoresist (60) on the hard mask insulation layer;

Selectively performing a photo-exposure process and a developing process to form a photoresist pattern having a first width for forming a line pattern (see figure 1);

Selectively etching the hard mask sacrificial layer by using the photoresist pattern as an etch mask to form a sacrificial hard mask having a second width (see figure 2);

Removing the photoresist pattern (see figure 3-4);

Etching the hard mask insulation layer (see figure 3) by controlling excessive etching conditions with use of the sacrificial hard mask as an etch mask to form a hard mask having a third width (see figure 3); and

Etching the etch target layer (see figure 4) by using the sacrificial hard mask and the hard mask as an etch mask to form the line pattern having a fourth width (see figure 4), wherein the first width (see figure 1) is wider than the fourth width (see figure 4).

Regarding to claims 2, 28, etch target layer is a conductive layer (polysilicon) and the line pattern is one of a bit line, a word line and a metal line (30).

Regarding to claims 6, 30, the sacrificial hard mask is removed at the step of removing etch target (conductive) layer (see figure 3-4).

Regarding to claims 9, 33, hard mask sacrificial layer is made of an oxide-based material, nitride-based material or an oxynitride based material (see col. 2, lines 62-65).

However, the reference does not teach forming an etch target (conductive) layer by using tungsten.

Aminpur et al. teaches forming an etch target (conductive) layer by using tungsten (515, see col. 5, lines 1-30, meeting claims 10, 26).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form the etch target layer by using tungsten in process of Huang or Chan or Ohuchi et al. as taught by Aminpur et al. because determining the optimum material for the layer only involved routine skill in the art.

Ohuchi et al. teaches forming a photoresist pattern by using ArF or F_2 photolithography (see col. 14, lines 42-54, meeting claim 4, 27)

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would form a photoresist pattern by using ArF or F_2 photolithography in process of Chan or Huang et al. because the process is known in developing photoresist pattern.

Nallan et al. teaches, regarding to claims 11, 17, 35, etching the tungsten layer by using a plasma containing a mixed gas of SF_6 and N_2 (abstract).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etching the tungsten layer using a plasma containing a mixed gas of SF_6 and N_2 in process of Chan or Huang et al. because the process would provide a better control etching profile of the tungsten layer.

Referring to figures 1-6, Blosse et al. teaches a method of forming a gate stack comprising: forming a target layer (26) on the oxide layer (24), forming a first and second mask layer (34/36) on the target layer, forming a organic anti-reflective layer (38) on the mask layer, and forming a photoresist layer (40) over the anti-reflective layer (see figure 1-10 and related text). Regarding to claim 24, etching the antireflective layer by using plasma containing mixed gas of Cl_2 and Ar (see col. 11, lines 47-56).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would to form an antireflective layer between the photoresist layer and the mask layer and etching it with plasma containing mixed gas of Cl_2 and Ar in process of Chan et al. as taught by Blosse et al. because the process would prevent the reflection light exposure.

The width range, power range, pressure range, and flowrate range are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious:

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the

general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any width range, power range, pressure range, and flowrate range suitable to the method in process of Huang et al. or Chan et al.in order to optimize the process.

Allowable Subject Matter

Claims4, 15-26, 20, 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800